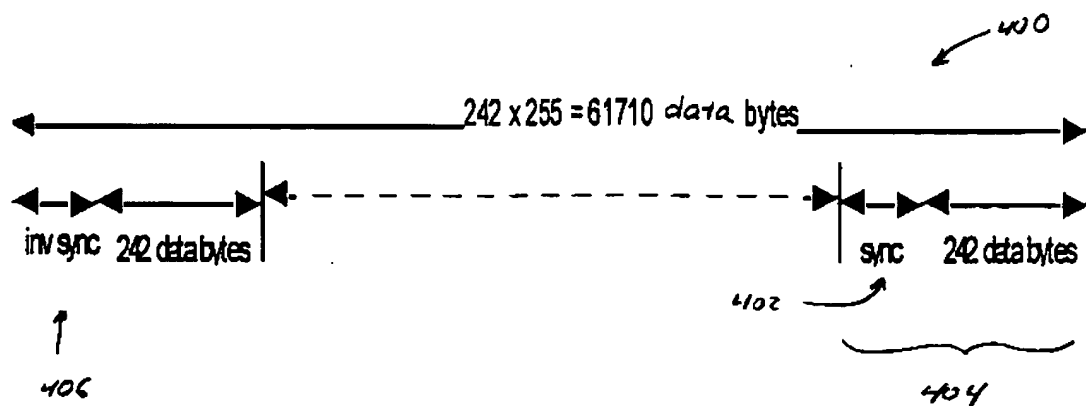


```

graph LR
    A[Packets from DSS source encoder] --> B[Super Frame Formatter 102]
    B --> C["RS(n,k) encoder GF(2^8) 104"]
    C --> D["Symbol interleaver (n,b) 106"]
    D --> E[Turbo sync insert 108]
    E --> F[Variable rate binary turbo enc. 110]
    F --> G[Bit to symbol mapper 112]
    G --> H[3/42-PSK modulator 114]
    H --> I[RF SIGNAL]
  
```



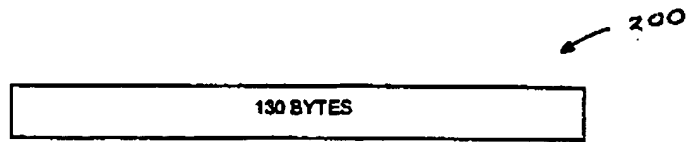


FIG. 2

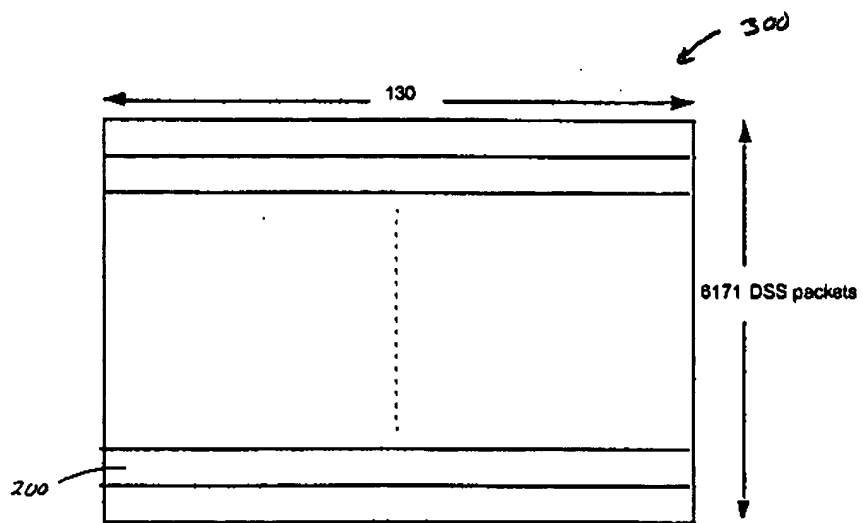


FIG. 3

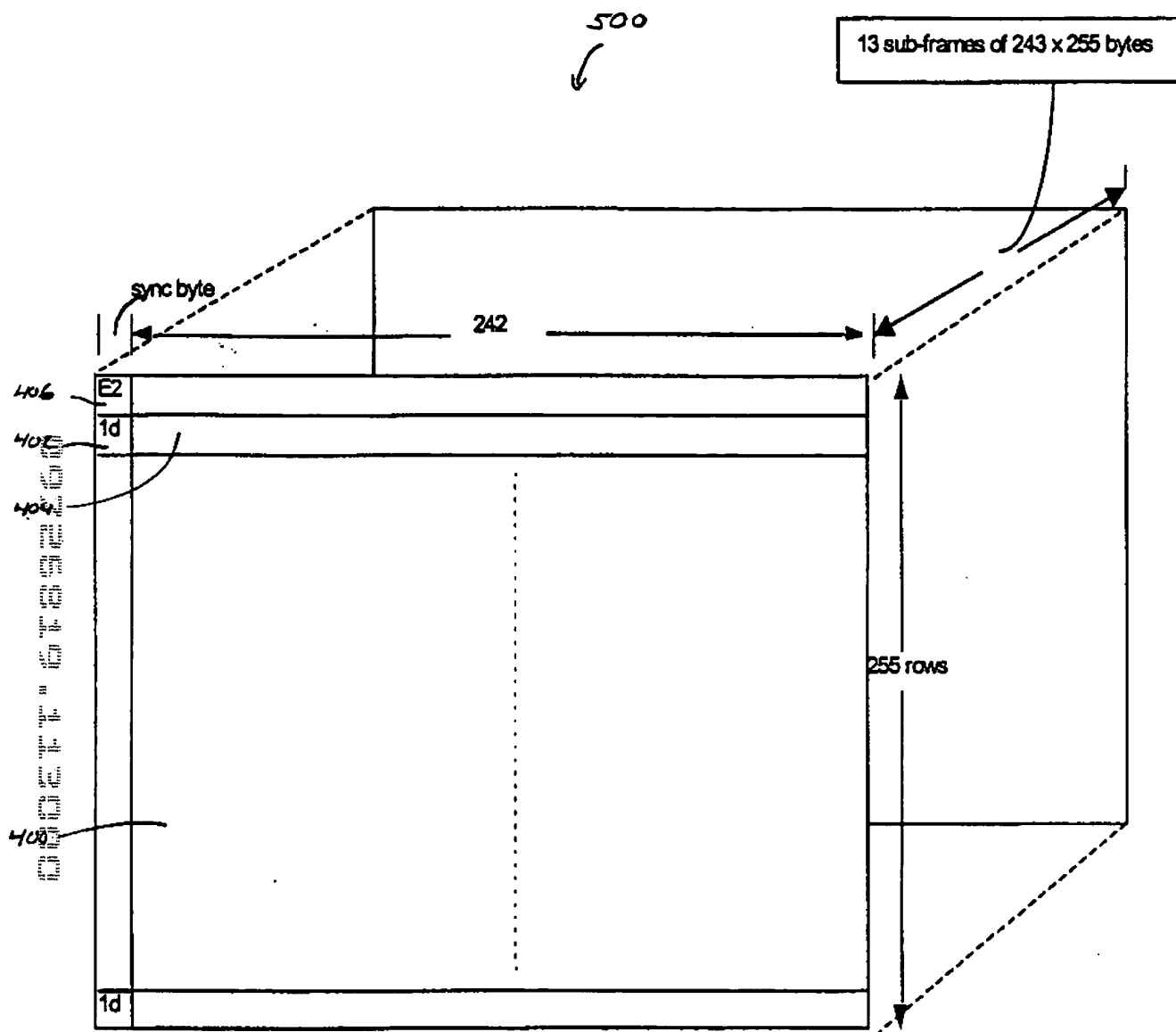


FIG. 5

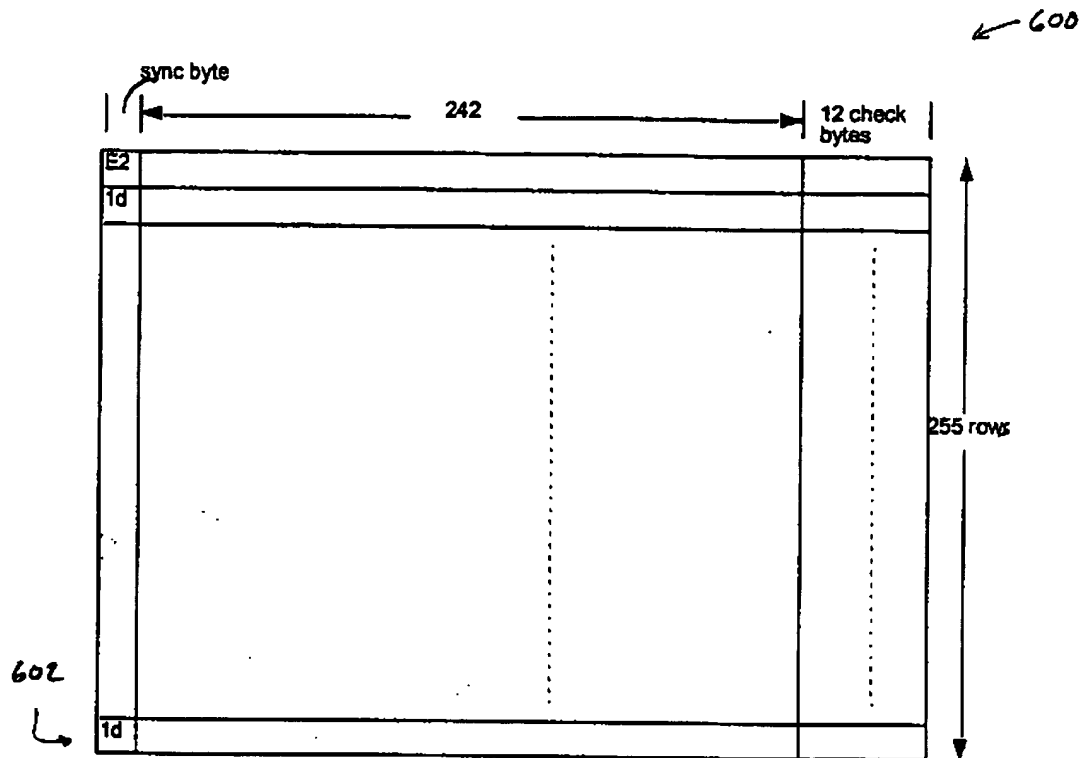


FIG. 6

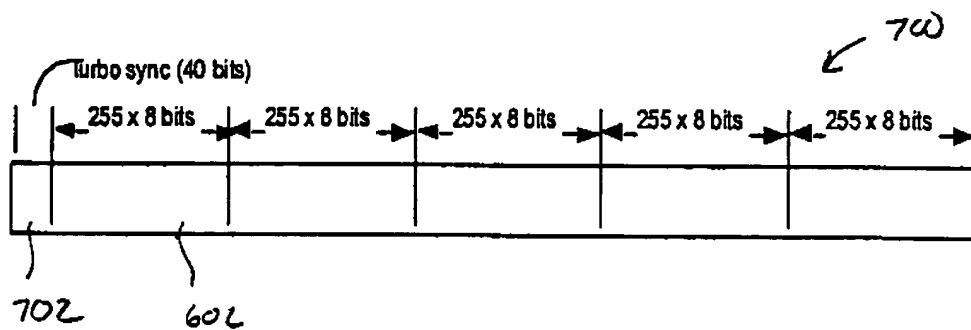


FIG. 7

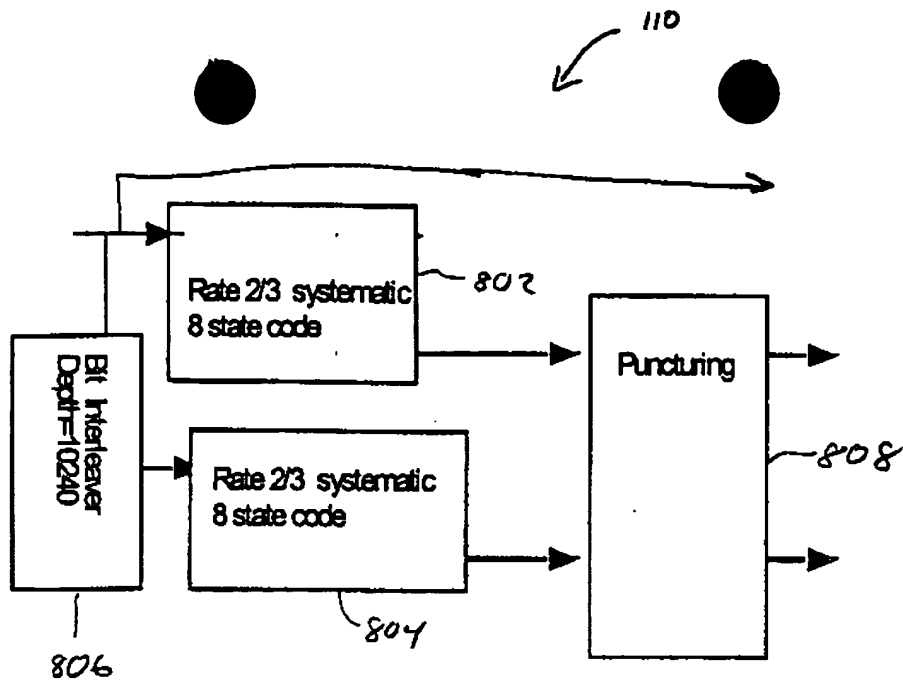


FIG. 8

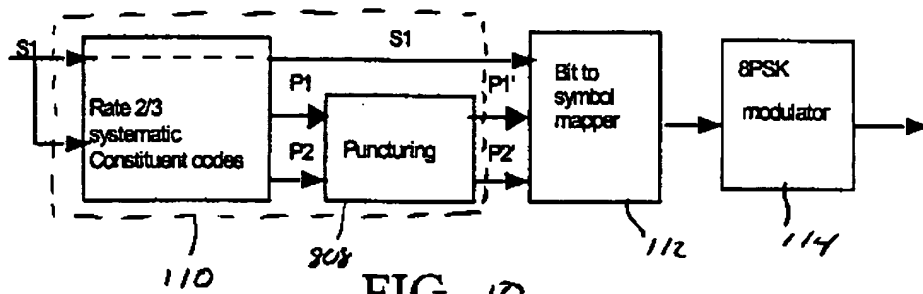


FIG. 10

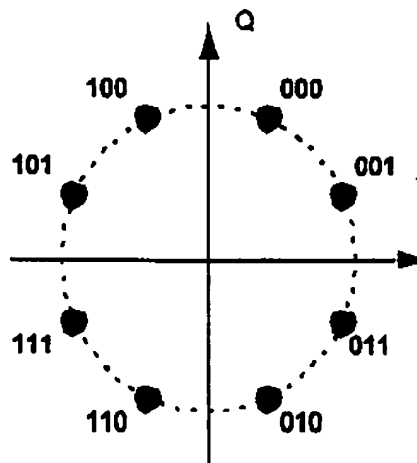


FIG. 11

FIG. 9a

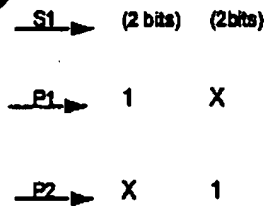


FIG. 9b

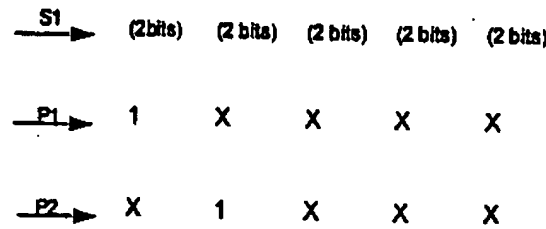


FIG. 9c

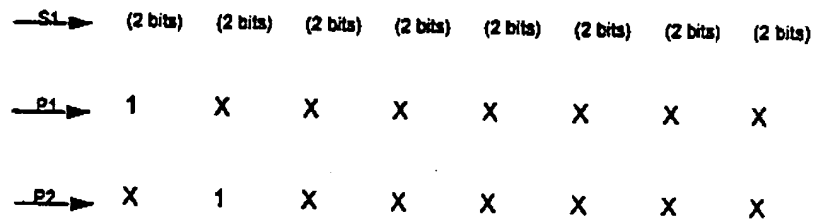


FIG. 9d

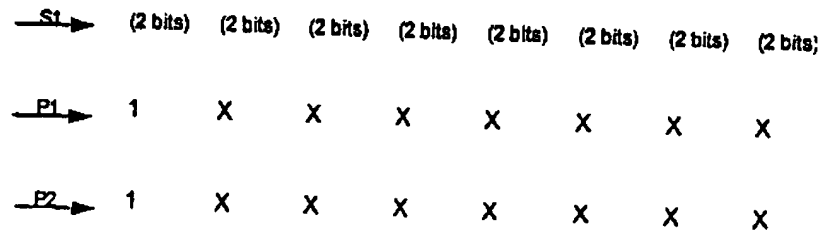
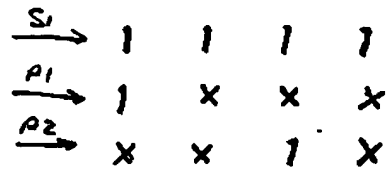


FIG. 9e



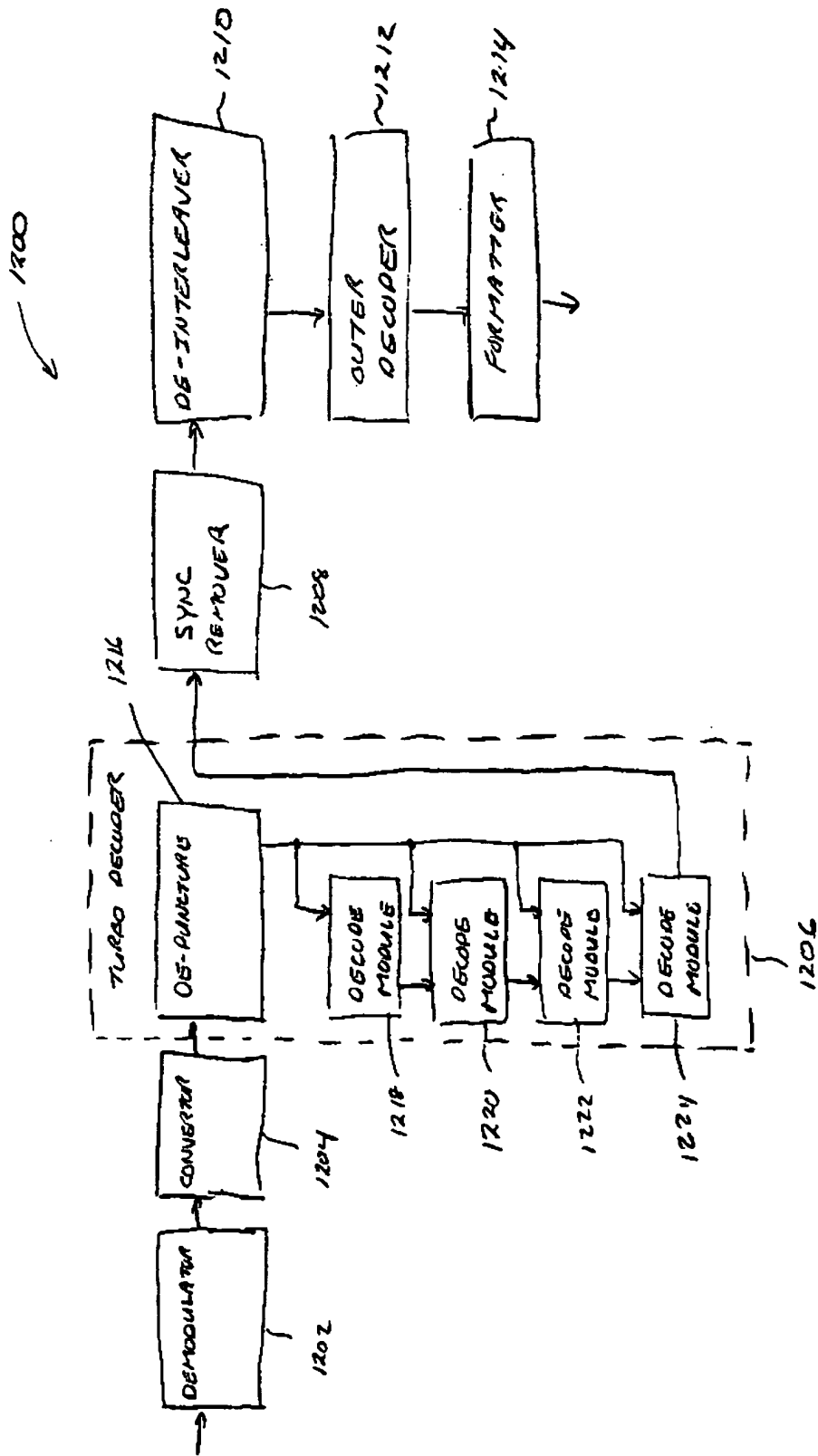


FIG. 12

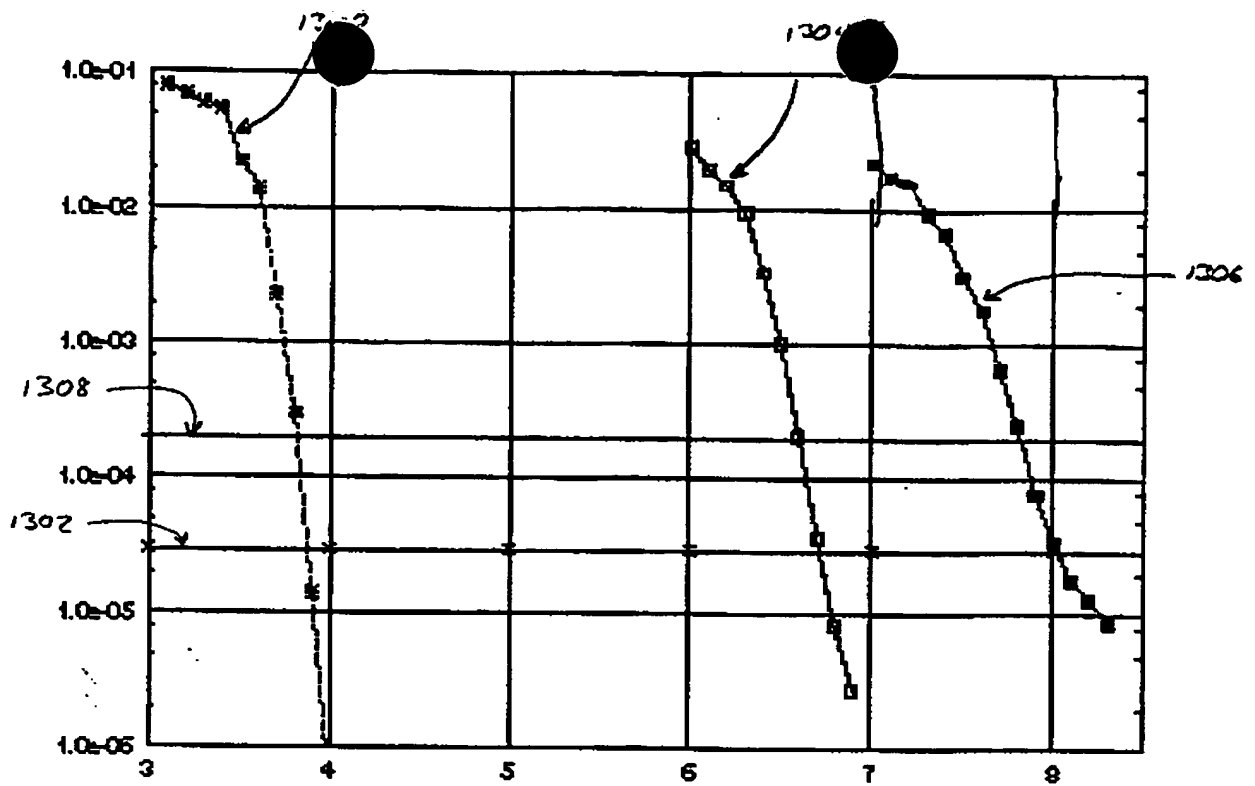


FIG. 13